

**Notice of Allowability**

Application No.

09/737,342

Examiner

Aimee J Li

Applicant(s)

MOORE ET AL.

Art Unit

2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Appeal Brief filed 24 January 2005.
2. ☒ The allowed claim(s) is/are 1-50 and 55-59 renumbered as 1-55.
3. ☐ The drawings filed on \_\_\_\_\_ are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☐ All    b) ☐ Some\*    c) ☐ None    of the:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
  6. ☒ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
    - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
    - (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08),  
Paper No./Mail Date \_\_\_\_\_
4. ☐ Examiner's Comment Regarding Requirement for Deposit  
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413),  
Paper No./Mail Date \_\_\_\_\_
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_

### EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.
2. Authorization for this examiner's amendment was given in a telephone interview with Richard Frankeny (Reg. No. 47,573) on 06 April 2005.
3. The application has been amended as follows:
  - a. Paragraphs to be added to the specification at the location indicated on the following pages.
  - b. Amend the claims as indicated on the following pages.
  - c. In addition to the claim amendments in (b), please make the following corrections:
    - i. Claim 1, lines 17-18 in the attached amendments states "...said second register matches said first register address". Please correct that to "...said second register address matches said first register address".
    - ii. Claim 26, lines 21-22 in the attached amendments states "...said second register matches said first register address". Please correct that to "...said second register address matches said first register address".
4. The following changes to the drawings have been approved by the examiner and agreed upon by applicant: Add Figure 14 as shown on the following pages. In order to avoid abandonment of the application, applicant must make these above agreed upon drawing changes.

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5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.
6. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.
7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL  
Aimee J. Li  
7 April 2005

  
EDDIE CHAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100

IN THE SPECIFICATION

Please add the following description of FIG. 14 which was added as suggested by the Examiner to make the drawings conform to the Specification and the Claims. Since FIG. 14 places elements found separately in FIGS. 1-6 and described in the Specification, the Applicants have added additional detailed description of added FIG. 14.

Please insert the following paragraphs beginning on page 33, line 21:

FIG. 14 is a block diagram of circuit elements described relative to FIGS. 1-13 and in particular to FIGS. 1-6. SRB 212 comprises a plurality of registers (in this case 64 registers). The registers are partitioned into a plurality of data entry fields: Valid bits 601, Instruction ID 602, Instruction Status 603, Load/Store 604, Real Address 605, and Quadword 607. Since there are 64 registers in SRB 212 there are 64 data entries in each data entry field (e.g., Real Address (0)-Real Address (63)). Address Generator generates the addresses 1516 used to access SRB 212. Data entries corresponding to register addresses (0-63) may be updated (add data) or removed (deleted). Registers of the SRB 212, according to embodiments of the present invention, are addressed by the use of pointers. Pointers contain the addresses of the registers in the SRB 212. Particular pointers, for example, the IN pointer 615 and the OUT pointer 614, are loaded with particular register addresses which are indexed under certain conditions. The IN pointer 615 points to the register where a register entry is next added and OUT pointer 614 points to the register where a register entry is next retired or removed.

Operations of the SRB are performed by special circuitry called filters. Filters, according to embodiments of the present invention, are uniquely associated with each service (operations that are performed on data entry fields). All filters operate in parallel, checking to determine whether there is any entry that needs the particular service of the filter, selecting the earliest entry if there are several, and dispatching that entry to the hardware that performs the service. The filters also perform the operation of "scanning" the entry fields of the SRB 212. Scanning may be done with a multiplexer or other circuit that allows a predetermined input value (e.g., a real address) to be compared to a

value in like data entry fields (e.g., Real Address fields 605 ) in the SRB 212 registers to determine a match. On a match, the address of the register containing the matching value is compared to the register addresses bounded by register address pointers (e.g., IN pointer 615 and OUT pointer 614). Operations may be performed on data entry fields of a register corresponding to a matching value as a result of scanning based on a decode of other data entry fields (e.g., Instruction Status field 605).

FIG. 14 illustrates circuitry employed in a filter. For example, Real Addresses 605 are coupled in parallel to multiplexer (MUX) 1511. A scan signal 1517 produces each Real Address (0-63) stored in data entry field 605 as a sequential output of MUX 1511. To determine if a particular Real Address 1514 is in SRB 212, comparator 1512 compares input Real Address 1514 to the scanned Real Addresses 605. In this example, MUX 1511 decodes addresses (0-63) to produce the required signals internal to MUX 1511 that sequentially selects the stored Real Addresses (0-63). If comparator 1512 determines the input Real Address 1514 matches with a stored Real Address 605, then a compare signal 1513 is generated that latches the scan signal value (register address corresponding to the compare 1513) into latch 1509 which is outputted as Match Address 1508. Match Address 1508 is the register address (0-63) which has the Real Address 605 that matches the input Real Address 1514. An address comparison circuit compares MA 1508 with IN Pointer (Ptr.) 615 (address) and the OUT Ptr. 614 (address) to determine if MA 1508 indicates that the register corresponding to MA 1508 is in a register whose address lies between IN Ptr. 615 and OUT Ptr. 614. Entries in registers between IN Ptr. 615 and OUT Ptr. 614 have valid entries as indicated by Valid bit 601.

If a Real Address 605 matches input Real Address 1514 and it is in a register located between IN Ptr. 615 and OUT Ptr. 614, then MA 1508 is outputted as gated MA 1504 to Address Generator 1505 which outputs the data entry fields of the register with the address corresponding to MA 1504. In this example, the Quadword 607 in the register (0-63) of SRB 212 corresponding to MA 1504 is dispatched to an operation unit (e.g., IMU 102) in response to a decode of data in the Instruction Status 603 entry by decoder 1503. Other operations may be done on data entry fields (e.g., 601-605) of a

register corresponding to a matching values as a result of scanning based on a decode of other data entry fields. Since the operations to be performed on data in each of the SRB registers is contained within the fields of the registers, the SRB has a "data flow" architecture. More detailed operations of the SRB are explained relative to the state diagrams of FIGS. 7-12. FIG 14 only shows scanning being implemented on the Real Address 605 data entry field. It is understood that any of the particular data entry fields shown in FIG 14 or other data entry fields not shown in this example of FIG. 14 may employ the data flow architecture with filters operating in parallel to scan the data entry fields.

Ravi Nair, et al.  
AUS9-2000-0001-US1

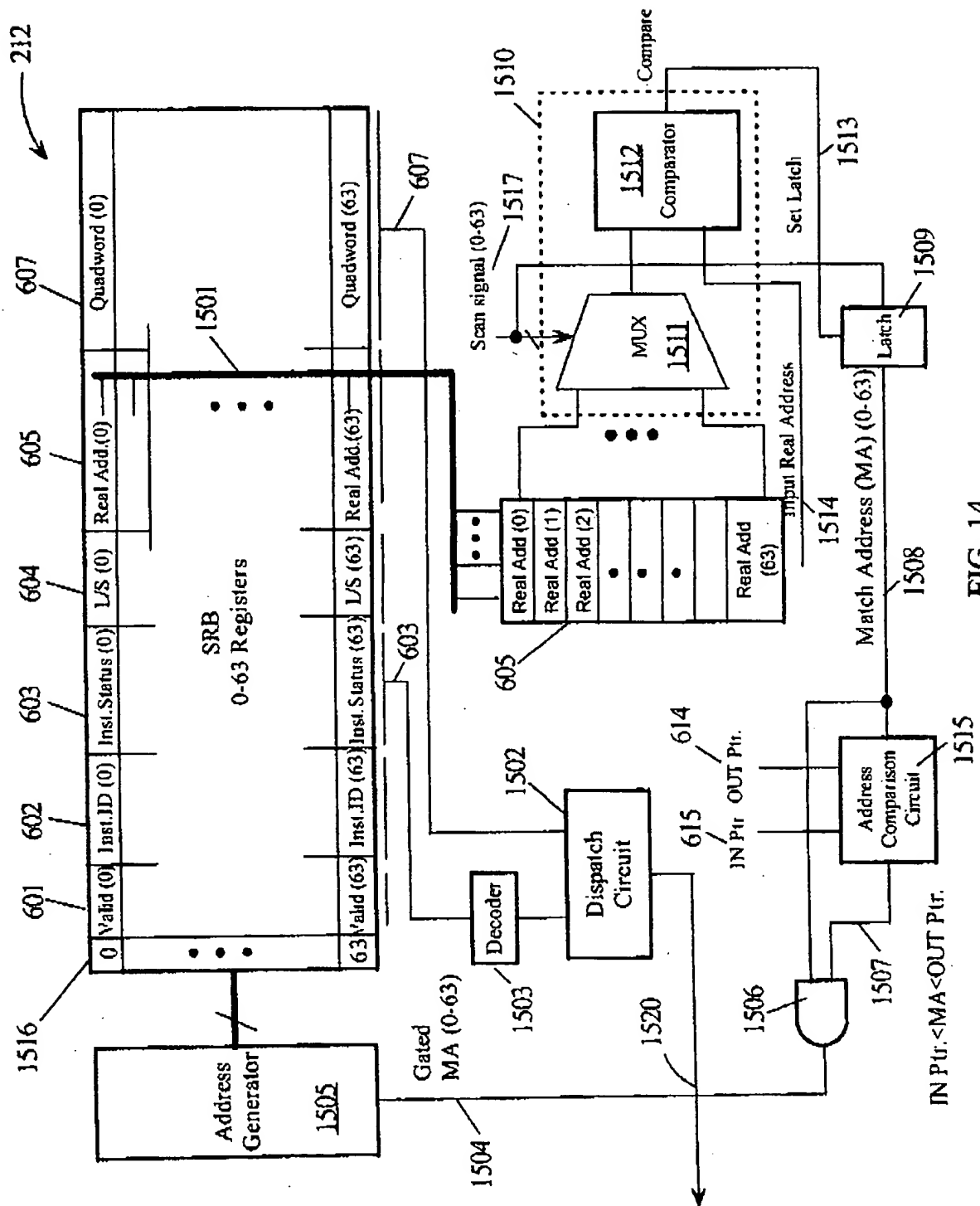


FIG. 14

IN THE CLAIMSListing of Claims:

1 1. (currently amended) An apparatus for managing operations in a processor, said  
2 apparatus comprising:

3 a plurality of addressable registers, each of said registers partitioned into plurality  
4 of data entry fields;

5 a first comparison circuit; ~~said first comparison circuit~~ operable to scan a like data  
6 entry field of said plurality of addressable registers and compare [[a]] data value in a set  
7 of said like data entry fields to [[a]] predetermined input data value;

8 a second comparison circuit; ~~said second comparison circuit~~ operable to compare  
9 a first register address of a first register in said plurality of addressable registers;  
10 ~~corresponding to a comparison match of said first comparison circuit~~; to a second register  
11 address of a second register in said plurality of addressable registers, wherein said first  
12 register address corresponds to a first register that has said data in said like data entry  
13 field that matches said predetermined input data; and

14 a dispatch circuit operable to dispatch data of a second data entry field of [[a]]  
15 said second register corresponding to said second register address to an operation unit in  
16 response to a decode of data in a third data entry field of said second register ~~and a~~  
17 ~~comparison match of~~ when said second comparison circuit indicates said second register  
18 matches said first register address.

1 2. (original) The apparatus of claim 1, wherein said operations are Load and Store  
2 operations within said processor.

1 3. (currently amended) The apparatus of claim 1, wherein said predetermined input  
2 ~~value~~ data is a real address requesting particular data corresponding to one of a Load and  
3 a Store operation.



1 4. (previously presented) The apparatus of claim 1, wherein said first comparison circuit  
2 comprises multiple like entry comparison circuits, each of said multiple like entry  
3 comparison circuits operable concurrently in parallel.

1 5. (original) The apparatus of claim 1, wherein said operation unit comprises an  
2 Instruction Management Unit (IMU).

1 6. (previously presented) The apparatus of claim 2, wherein said operation unit  
2 comprises a Storage Management Unit (SMU) said SMU comprising data cache memory  
3 and controller and a Storage Reference Buffer (SRB).

1 7. (original) The apparatus of claim 1, wherein one of said data entry fields is a Valid bit  
2 field, said Valid bit field indicating whether other data entry fields are valid.

1 8. (original) The apparatus of claim 1, wherein one of said data entry fields is an  
2 Instruction Identification (ID) field corresponding to a particular Load and Store  
3 operation.

1 9. (original) The apparatus of claim 1, wherein one of said data entry fields is an  
2 Instruction status field corresponding to a status of one of said Load and Store operations.

1 10. (original) The apparatus of claim 1, wherein one of said data entry fields is a  
2 Load/Store field having a Load/Store bit, said Load/Store bit corresponding to a Load  
3 operation if said Load/Store bit has a first logic state and corresponding to a Store  
4 operation if said Load/Store bit has a second logic state.

1 11. (original) The apparatus of claim of claim 1, wherein one of said data entry fields  
2 comprises Real Address field, said Real Address field corresponding to a particular Real  
3 Address of memory data.

1 12. (original) The apparatus of claim 1, wherein one of said data entry fields is a  
2 Quadword field, said Quadword field comprising multiple bytes of data.

1 13. (original) The apparatus of claim 1, wherein one of said data entry fields is an  
2 Operand Mask field, said Operand Mask field defining selected bytes of data within a  
3 selected one of said data entry fields.

1 14. (original) The apparatus of claim 1, wherein said operation unit is a pipeline  
2 execution unit operating concurrently on a plurality of said data entry fields.

1 15. (original) The apparatus of claim 1, wherein said addressable registers are addressed  
2 using a plurality of address pointers.

1 16. (previously presented) The apparatus of claim 6 wherein said addressable registers  
2 are configured as said Storage Reference Buffer (SRB).

1 17. (original) The apparatus of claim 15, wherein one of said address pointers is a third  
2 pointer, said third pointer, said third pointer pointing to one of said addressable registers  
3 whose data entry fields contain data defining an earliest Store operation that is either  
4 unresolved or that matches a register address of a current Load operation.

1 18. (original) The apparatus of claim 15, wherein said address pointers comprise a  
2 fourth and a fifth pointer, said fourth and fifth pointers defining a window of register  
3 addresses from which a Load operation may be satisfied without having to access other  
4 memory storage.

1 19. (original) The apparatus of claim 15, wherein said second register address is selected  
2 from registers addresses which fall within a window of register addresses, said window  
3 of addresses defined by said address pointers.

1 20. (original) The apparatus of claim 15, wherein one of said address pointers is a first  
2 pointer, said first pointer pointing to an IN register address of a first available register  
3 into which data may be added.

1 21. (original) The apparatus of claim 15, wherein one of said address pointers is a  
2 second pointer, said second pointer pointing to an OUT register address of a first  
3 available register from which register data may be retired.

1 22. (original) The apparatus of claim 16, wherein said data entry fields, added to said  
2 SRB after a mis-predicted branch instruction occurs in said processor, are retired and said  
3 first pointer is indexed to first register address of a register with added register data entry  
4 bits which were added immediately prior to said mis-predicted branch instruction.

1 23. (original) The apparatus of claim 19, wherein said window of register addresses  
2 defines active Load and Store operations.

1 24. (original) The apparatus of claim 20, wherein said first pointer is indexed by one  
2 when said register data has been added, said first pointer having a minimum and a  
3 maximum value wherein a decrement down from a minimum value results in said  
4 maximum value and an increment up from said maximum value results in said minimum  
5 value.

1 25. (original) The apparatus of claim 21, wherein said second pointer is indexed by one  
2 when register entry bits have been deleted, said second pointer having a minimum and a  
3 maximum value wherein a decrement down from said minimum value results in said  
4 maximum value and an increment up from said maximum value results in said minimum  
5 value.

1 26. (currently amended) A data processing system, comprising:  
2 a central processing unit (CPU);  
3 random access memory (RAM);  
4 read only memory (ROM);  
5 an I/O adapter; and  
6 a bus system coupling devices internal to said CPU, said CPU comprising an  
7 apparatus for managing operations within a processor of said CPU, said apparatus  
8 comprising:

9 a first comparison circuit, ~~said first comparison circuit~~ operable to scan a like data  
10 entry field of said plurality of addressable registers and compare [[a]] data value in a set  
11 of said like data entry fields to [[a]] predetermined input data value;

12 a second comparison circuit, ~~said second comparison circuit~~ operable to compare  
13 a first register address of a first register in said plurality of addressable registers;  
14 corresponding to a comparison match of said first comparison circuit; to a second register  
15 address of a second register in said plurality of addressable registers, wherein said first  
16 register address corresponds to a first register that has said data in said like data entry  
17 field that matches said predetermined input data; and

18 a dispatch circuit operable to dispatch data of a second data entry field of [[a]]  
19 said second register corresponding to said second register address to an operation unit in  
20 response to a decode of data in a third data entry field of said second register ~~and a~~  
21 ~~comparison match of~~ when said second comparison circuit indicates said second register  
22 matches said first register address.

1 27. (original) The data processing system of claim 26, wherein said operations are Load  
2 and Store operations within said processor.

1 28. (currently amended) The data processing system of claim 26, wherein said  
2 predetermined input ~~value~~ data is a real address requesting particular data corresponding  
3 to one of a Load and a Store operation.

1 29. (previously presented) The data processing system of claim 26, wherein said first  
2 comparison circuit comprises multiple like entry comparison circuits, each of said  
3 multiple like entry comparison circuits operable concurrently in parallel.

1 30. (original) The data processing system of claim 26, wherein said operation unit  
2 comprises an Instruction Management Unit (IMU).

1 31. (previously presented) The data processing system of claim 27, wherein said  
2 operation unit comprises a Storage Management Unit (SMU) said SMU comprising data  
3 cache memory and controller and a Storage Reference Buffer (SRB).

1 32. (original) The data processing system of claim 26, wherein one of said data entry  
2 fields is a Valid bit field, said Valid bit field indicating whether other data entry fields are  
3 valid.

1 33. (original) The data processing system of claim 26, wherein one of said data entry  
2 fields is an Instruction Identification (ID) field corresponding to a particular Load and  
3 Store operation.

1 34. (original) The data processing system of claim 26, wherein one of said data entry  
2 fields is an Instruction status field corresponding to a status of one of said Load and Store  
3 operations.

1 35. (original) The data processing system of claim 26, wherein one of said data entry  
2 fields is a Load/Store field having a Load/Store bit, said Load/Store bit corresponding to  
3 a Load operation if said Load/Store bit has a first logic state and corresponding to a Store  
4 operation if said Load/Store bit has a second logic state.

1 36. (original) The data processing system of claim of claim 26, wherein one of said data  
2 entry fields comprises Real Address field, said Real Address field corresponding to a  
3 particular Real Address of memory data.

1 37. (original) The data processing system of claim 26, wherein one of said data entry  
2 fields is a Quadword field, said Quadword field comprising multiple bytes of data.

1 38. (original) The data processing system of claim 26, wherein one of said data entry  
2 fields is an Operand Mask field, said Operand Mask field defining selected bytes of data  
3 within a selected one of said data entry fields.

1 39. (original) The data processing system of claim 26, wherein said operation unit is a  
2 pipeline execution unit operating concurrently on a plurality of said data entry fields.

1 40. (original) The data processing system of claim 26, wherein said addressable registers  
2 are addressed using a plurality of address pointers.

1 41. (previously presented) The data processing system of claim [[26]] 31 wherein said  
2 addressable registers are configured as said Storage Reference Buffer (SRB).

1 42. (original) The data processing system of claim 40, wherein one of said address  
2 pointers is a third pointer, said third pointer, said third pointer pointing to one of said  
3 addressable registers whose data entry fields contain data defining an earliest Store  
4 operation that is either unresolved or that matches a register address of a current Load  
5 operation.

1 43. (original) The data processing system of claim 40, wherein said address pointers  
2 comprise a fourth and a fifth pointer, said fourth and fifth pointers defining a window of  
3 register addresses from which a Load operation may be satisfied without having to access  
4 other memory storage.

1 44. (original) The data processing system of claim 40, wherein said second register  
2 address is selected from registers addresses which fall within a window of register  
3 addresses, said window of addresses defined by said address pointers.

1 45. (original) The data processing system of claim 40, wherein one of said address  
2 pointers is a first pointer, said first pointer pointing to an IN register address of a first  
3 available register into which data may be added.

1 46. (original) The data processing system of claim 40, wherein one of said address  
2 pointers is a second pointer, said second pointer pointing to an OUT register address of a  
3 first available register from which register data may be retired.

1 47. (original) The data processing system of claim 41, wherein said data entry fields,  
2 added to said SRB after a mis-predicted branch instruction occurs in said processor, are  
3 retired and said first pointer is indexed to first register address of a register with added  
4 register data entry bits which were added immediately prior to said mis-predicted branch  
5 instruction.

1 48. (original) The data processing system of claim 44, wherein said window of register  
2 addresses defines active Load and Store operations.

1 49. (original) The data processing system of claim 45, wherein said first pointer is  
2 indexed by one when said register data has been added, said first pointer having a  
3 minimum and a maximum value wherein a decrement down from a minimum value  
4 results in said maximum value and an increment up from said maximum value results in  
5 said minimum value.

1 50. (original) The data processing system of claim 46, wherein said second pointer is  
2 indexed by one when register entry bits have been deleted, said second pointer having a  
3 minimum and a maximum value wherein a decrement down from said minimum value  
4 results in said maximum value and an increment up from said maximum value results in  
5 said minimum value.

1 55. (previously presented) The apparatus of claim 6, wherein the SRB comprises the  
2 plurality of addressable registers.

1 56. (previously presented) The apparatus of claim 55, wherein a Load operation in one  
2 of the Load and Store operations comprises:  
3 issuing concurrently a fetch instruction requesting a real address to a data cache  
4 and the Storage Reference Buffer (SRB), the real address corresponding to an address of  
5 multiple bytes of data;  
6 scanning the addressable registers in the SRB for the real address;  
7 receiving the multiple bytes of data from the SRB if the real address is available;  
8 retrieving the multiple bytes of data first from the SRB if the real address is  
9 available and second from the data cache if the real address is not available in the SRB;  
10 and  
11 updating a corresponding one of the addressable registers with the multiple bytes  
12 of data.

1 57. (previously presented) The apparatus of claim 55, wherein a Store operation in one  
2 of the Load and Store operations comprises:

- 3 issuing a real address generation instruction;
- 4 looking up the real address in a table lookup buffer;
- 5 sending the real address to a miss resolution processor if the real address is not in  
6 the table lookup buffer, the miss resolution processor determining a translated real  
7 address;
- 8 sending the real address from one of the miss resolution processors and the table  
9 lookup buffer to the SRB; and
- 10 updating corresponding data entry fields in one of the addressable registers in the  
11 SRB.

1 58. (previously presented) The apparatus of claim 55, wherein a Store operation in one  
2 of the Load and Store operations comprises:

- 3 issuing an address generation instruction by a first instruction unit generating a  
4 real address in memory;
- 5 updating the real address in a real address field of one of the addressable registers  
6 in the SRB;
- 7 sending concurrently, a request for a multiple byte word with the real address to  
8 the SRB and a data cache;
- 9 receiving the multiple byte word from one of the addressable registers in the  
10 Storage Reference Buffer and from a data cache;
- 11 updating the multiple byte word from the data cache with an operand mask;
- 12 receiving from the first instruction unit store data operand;
- 13 aligning the store data operand to the multiple bytes of data; and
- 14 updating the multiple bytes of data with a complement of the operand mask.

1 59. (previously presented) The apparatus of claim 55, wherein a Load operation in one  
2 of the Load and Store operations comprises:



3           issuing an address generation instruction by a first instruction unit generating a  
4   real address in a memory;  
5           updating the real address in a real address field of one of the addressable registers  
6   in the SRB;  
7           sending concurrently, a request for a multiple byte word with the real address to  
8   the SRB and a data cache;  
9           receiving the multiple byte word from one of the addressable registers in the SRB  
10   and the data cache;  
11          extracting selected bytes from the multiple byte word;  
12          receiving the selected bytes by the first instruction unit; and  
13          updating the multiple bytes of data with a complement of the operand mask.